Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	30	("first power rail") and ("second power rail")	US-PGPUB	OR	OFF	2005/09/14 13:47
L2	3	("first power rail") and ("second power rail") and latch and "clock signal"	US-PGPUB	OR	OFF	2005/09/14 13:44
L3	4	("first power rail") and ("second power rail") and ("third power rail")	US-PGPUB	OR	OFF	2005/09/14 13:46

DB = East

examiner initial: EA

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	10432	((stress adj2 test$3) or (burn-in adj2 test$3))	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 13:52
L7	76	((stress adj2 test$3) or (burn-in adj2 test$3) or (stress$3 adj3 (device or IC or circuit))) and (power adj3 rail$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 13:56
L8	7	((stress adj2 test$3) or (burn-in adj2 test$3) or (stress$3 adj3 (device or IC or circuit))) and (power adj3 rail$1) and latch$3 and (clock adj2 signal$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:04
L9	76	((stress adj2 test$3) or (burn-in adj2 test$3) or (stress$3 adj3 (device or IC or circuit))) and (power adj3 rail$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:05
L10	0	((stress adj2 test$3) or (burn-in adj2 test$3) or (stress$3 adj3 (device or IC or circuit))) and (power adj3 rail$1) and 714/726.ccls.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:05
L11	1	((stress adj2 test$3) or (burn-in adj2 test$3) or (stress$3 adj3 (device or IC or circuit))) and (power adj3 rail$1) and 326/16.ccls.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:06
L12	10	(first adj2 power adj2 rail$1) and (second adj2 power adj2 rail) and latch$3 and (clock adj2 signal$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:08
L13	5	(first adj2 power adj2 rail$1) and (second adj2 power adj2 rail) and latch$3 and (clock adj2 signal$1) and test$4	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:13
L14	5	(first adj2 power adj2 rail$1) and (second adj2 power adj2 rail) and (latch$3 or flip-flop$) and (clock adj2 signal$1) and test$4	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:09
L15	3	(first adj2 power adj2 rail$1) and (second adj2 power adj2 rail) and (latch$3 or flip-flop$) and (clock adj2 signal$1) and test$4 and overlap$6	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:10
L16	4	(first adj2 power adj2 rail$1) and (second adj2 power adj2 rail) and (first adj2 (latch or flip-flop or ff)) and (second adj2 (latch or flip-flop or ff))	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:14

L17	1	(first adj2 power adj2 rail$1) and (second adj2 power adj2 rail) and (first adj2 (latch or flip-flop or ff)) and (second adj2 (latch or flip-flop or ff)) and (clock adj2 signal)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:15
L18	1	(first adj2 power adj2 rail$1) and (second adj2 power adj2 rail) and (first adj2 (latch or flip-flop or ff)) and (second adj2 (latch or flip-flop or ff)) and (test$3 or stress$4 or burn-in)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:16
L19	111	(first adj2 power) and (second adj2 power) and (first adj2 (latch or flip-flop or ff)) and (second adj2 (latch or flip-flop or ff)) and (test$3 or stress$4 or burn-in)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:16
L20	46	(first adj2 power) and (second adj2 power) and (first adj2 (latch or flip-flop or ff)) and (second adj2 (latch or flip-flop or ff)) and (first adj2 clock adj2 signal) and (second adj2 clock adj2 signal)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:17
L21	17	(first adj2 power) and (second adj2 power) and (first adj2 (latch or flip-flop or ff)) and (second adj2 (latch or flip-flop or ff)) and (first adj2 clock adj2 signal) and (second adj2 clock adj2 signal) and (test$4 or stress$4 or burn-in)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:24
L22	1	(first adj2 power) and (second adj2 power) and (first adj2 (latch or flip-flop or ff)) and (second adj2 (latch or flip-flop or ff)) and (first adj2 clock adj2 signal) and (second adj2 clock adj2 signal) and (test$4 or stress$4 or burn-in) and 714/726.ccls.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:18
L23	0	(first adj2 power) and (second adj2 power) and (first adj2 (latch or flip-flop or ff)) and (second adj2 (latch or flip-flop or ff)) and (first adj2 clock adj2 signal) and (second adj2 clock adj2 signal) and (test$4 or stress$4 or burn-in) and 326/16.ccls.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:19
L24	0	(first adj2 power) and (second adj2 power) and (first adj2 (latch or flip-flop or ff)) and (second adj2 (latch or flip-flop or ff)) and (first adj2 clock adj2 signal) and (second adj2 clock adj2 signal) and (test$4 or stress$4 or burn-in) and de-power$3	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:20

L25	2	(first adj2 power) and (second adj2 power) and (first adj2 (latch or flip-flop or ff)) and (second adj2 (latch or flip-flop or ff)) and (first adj2 clock adj2 signal) and (second adj2 clock adj2 signal) and (test$4 or stress$4 or burn-in) and overlap$6	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:21
L26	4	(stress$3 near3 (IC or (integrated circuit))) and 714/726.ccls.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:26
L27	13	((stress$3 near3 (IC or (integrated circuit))) or (stress adj2 test$3)) and 714/726.ccls.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:27
L28	0	((stress$3 near3 (IC or (integrated circuit))) or (stress adj2 test$3)) and 714/726.ccls. and (power adj3 rail$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:39
L29	35	bernstein-kerry.in.	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:44
L33	2	bernstein-kerry.in. and (stress near2 test$3)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:44
L34	5	bernstein-kerry.in. and (test$3)	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:46
L35	0	bernstein-kerry.in. and "power rail"	USPAT; EPO; JPO; DERWENT	OR	OFF	2005/09/14 14:46

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